## CLAIMS

What is claimed is:

1. A network processor comprising:

a plurality of standard cells; and

at least one field programmable gate array (FPGA) cell that can communicate with at least one of the standard cells, wherein the FPGA cell allows for customization of the network processor.

2. The network processor of claim 1, wherein the at least one FPGA cell can provide a specified function based upon field programming techniques to allow for customization of the network processor.

3. The network processor of claim 1 wherein the plurality of standard cells are utilized for common logic and the at least one FPGA cell is utilized for high risk logic.

4. A method for customizing a network processor; comprising the steps of:

(a) providing at least one field programmable gate array (FPGA) cell within the network processor;

(b) providing a custom logic file for the vendor of the network processor by a customer of the network processor; and

(c) programming the at least one FPGA cell, the vendor based upon the custom logic bill to provide a customized network processor.

5. The method of claim 4 wherein step (b) further comprises (b1) providing a verification module within the custom logic file.

6. The method of claim 4 which includes step (c) verifying the customized network processor based upon the verification module.

7. A network processor comprising:

a plurality of standard cells, the plurality of standard cells comprising common logic;

a plurality of FPGA cells, the plurality of FPGA cells comprising high risk logic; and

at least one bus coupled to a portion of the standard cells and portion of the FPGA cells, wherein each of the plurality of FPGA cells allows for customization of the network processor.

8. The network processor of claim 7, wherein the plurality of cells each can provide a specified function based upon field programming techniques to allow for customization of the network processor.

9. The network processor of claim 7 wherein the at least one bus comprises a processor local bus (PLB) and two on-chip peripheral buses (OPBs).

10. The network processor of claim 9 wherein the FPGA cells coupled to the PLB comprise an accelerator function and a PLB master/slave function.

11. The network processor of claim 9 wherein the FPGA cells coupled to one of the two OPBs are media interfaces.

12. The network processor of claim 9 wherein the FPGA cells coupled to the other of the two OPBs are a GPIO preprocessor function and an OPB master/slave function.

13. A network processor comprising:

a plurality of standard cells, the plurality of standard cells comprising common logic;

a plurality of FPGA cells, the plurality of FPGA cells comprising high risk logic; and

a processor local bus (PLB) and two on-chip peripheral buses (OPBs) coupled to a portion of the standard cells and portion of the FPGA cells, wherein the FPGA cells coupled to the PLB comprise an accelerator function and a PLB master/slave function; wherein the FPGA cells coupled to one of the two OPBs are media interfaces; wherein the FPGA cells coupled to the other of the two OPBs are a GPIO preprocessor function and an OPB master/slave function; wherein the plurality of cells each can provide a specified function based upon field programming techniques to allow for customization of the network processor.